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PTO/SB/21 (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	09/982,459
Filing Date	October 17, 2001
First Named Inventor	Ralf M. Schmitt
Art Unit	2825
Examiner Name	Annette M. Thompson
Total Number of Pages in This Submission	
Attorney Docket Number	SUN-P5405

ENCLOSURES ***(check all that apply)***

- ☒ Fee Transmittal Form
  - ☐ Fee Attached
- ☒ Amendment / Reply
  - ☒ After Final
  - ☐ Affidavits/declaration(s)
- ☒ Extension of Time Request
- ☐ Express Abandonment Request
- ☒ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☒ Drawing(s) (Replacement sheets)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☒ Terminal Disclaimer
- ☒ Request Continued Examination (RCE)
- ☐ CD, Number of CD(s) ____
- ☐ After Allowance Communication to Group
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to Group **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosure(s) *(please identify below)*:
  1449 citing 25 pieces of art
  Limited Recognition Under 37 CFR §10.9(b)

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Masako Ando, Limited Recognition Under 37 CFR §10.9(b)
Signature	Masako Ando
Date	5/13/04

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

Typed or printed name	Carol Diez		
Signature	Carol Diez	Date	5-13-04

PTO/SB/17 (10-03)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 1098

Complete If Known	
Application Number	09/982,459
Filing Date	October 17, 2001
First Named Inventor	Ralf M. Schmitt
Examiner Name	Annette M. Thompson
Art Unit	2825
Attorney Docket No.	SUN-P5405

METHOD OF PAYMENT *(check all that apply)*

☒ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☐ Deposit Account:

Deposit Account Number: 50-1698

Deposit Account Name: Thelen Reid & Priest, LLP

The Director is authorized to: *(check all that apply)*
☐ Charge fee(s) indicated below ☒ Credit any overpayments
☒ Charge any additional fee(s) during the pendency of this application
☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filling fee	

SUBTOTAL (1) ($) 0

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

			Extra Claims		Fee from below	=	Fee Paid
Total Claims	42	-36 **	6	X	18	=	108
Independent Claims	3	-3 **	0	X	86	=	0
Multiple Dependent				X		=	0

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 108

**or number previously paid, if greater; For Reissues, see above*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	110
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive – unavoidable	
1453	1,330	2453	665	Petition to revive – unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17 (q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR § 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	770
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) 1814 Terminal Disclaimer 110

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 990

SUBMITTED BY				Complete *(if applicable)*	
Name (Print/Type)	Masako Ando	*Registration No. (Attorney/Agent)*	LR37CFR10.9b	*Telephone*	(408) 292-5800
Signature	Masako Ando			*Date*	5/13/04

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/982,452	10/17/2001	Manjunath D. Haritsa	SUN-P5403	7441

7590 02/27/2003

David B. Ritchie
Thelen Reid & Priest LLP
P.O. Box 640640
San Jose, CA 95164-0640

EXAMINER
TAT, BINH C

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 02/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

EXCEL CPI

CIP
EXCEL
MAIL LOG

	Application No.	Applicant(s)	
Office Action Summary	09/982,452	HARITSA ET AL.	
	Examiner	**Art Unit**	
	Binh C. Tat	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-77* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-77* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2, 3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This office action is in response to application 09/982452 filed on 10/17/01.

Claims 1-77 remain pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-77 are rejected under 35 U.S.C. 102(b) as being anticipated by Naganuma et al. (U.S Patent 5917729).

3. As to claim 1 (method), 16 (apparatus), 31 (apparatus), and 43 (computer readable medium), Naganuma et al. teaches a method of determining clock insertion delays for a microprocessor design having grid-based clock distribution, the method comprising: partitioning the complete clock net into a global clock net and a plurality of local clock nets (see fig 5 col 7 lines 54-57 and fig 15 col 10 lines 20-23); simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net (see fig1 element ST10 and fig29 element ST21 and ST13 col 10 lines 55-68); simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets (see fig 1 element ST10 and fig29 element ST21 and ST13 col 10 lines 23-53); and combining the plurality of simulations to form the complete clock net (see fig 1 element ST10 and fig29 element ST21 and ST11-14 col 12 lines 36-41).

4. As to claims 2, 17, 32 and 44, Naganuma et al. teaches wherein partitioning comprises breaking the complete clock net into a plurality of parts approximating rectangular grid coordinates (see fig 2).

5. As to claims 3, 18, 33, and 45 Naganuma et al. teaches further comprising breaking at least one of the plurality of local clock nets down into at least one sub-local clock net (see fig 15 and fig 16).

6. As to claim 4, 19, 34 and 46, Naganuma et al. teaches further comprising simulating the at least one sub-local clock net prior to simulating the corresponding local clock net (see fig 1 element ST10 and fig29 element ST21 and ST13 col 10 lines 55-68).

7. As to claims 5, 20, 35, and 47, Naganuma et al. teaches wherein at least two of the plurality of local clock nets are simulated in parallel (see fig 1 element ST10 and fig29 element ST21 and ST13 col 10 lines 55-68).

8. As to claims 6, 21, 36, and 48, Naganuma et al. teaches wherein simulating each of the plurality of local clock nets comprises: extracting a layout of the local clock net and the conductors routed above and through the local clock net from a microprocessor network database (see fig 1 element ST10 and fig 29 element ST20 and ST13 col 12 lines 35-41); extracting component values of the elements of the local clock net from the microprocessor network database (see fig 1 element ST10 and fig29 element ST20 and ST13 col 12 lines 35-41); simulating the local clock net based on the layout and the component values (see fig 1 element ST10 and fig29 element ST21 and ST13 col 12 lines 35-41); and extracting a load of the local clock net on the global clock net (see fig 1 element ST10 and fig29 element ST21 and ST13 col 12 lines 35-41).

9. As to claims 7, 22, 37, and 49, Naganuma et al. teaches wherein simulating the local clock net comprises assuming that the clock arrival times from the global clock net will be simultaneous at all points where the local clock net is connected to the global clock net (see fig 1 element ST10 and fig29 element ST21 and ST13 col 12 lines 35-41).

10. As to claims 8, 23, 38, and 50, Naganuma et al. teaches wherein simulating the global clock net comprises: extracting the layout of the global clock net from a microprocessor network database (see fig 1 element ST10 and fig 29 element ST20 and ST13 col 12 lines 35-41 and col 10 lines 23-53); extracting component values of the elements of the global clock net from the microprocessor network database (see fig 1 element ST10 and fig 29 element ST20 and ST13 col 12 lines 35-41 and col 10 lines 23-53); inserting the simulated loads of the plurality of local clock nets (see fig 1 element ST10 and fig 29 element ST20 and ST13 col 12 lines 35-41); and simulating the global clock net based on the layout, the component values, and the simulated local clock net loads (see fig 1 element ST10 and fig29 element ST21 and ST13 col 12 lines 35-41).

11. As to claims 9, 24, 39, and 51, Naganuma et al. teaches further comprising storing the plurality of simulation results in a Clock Data Model (see col 12 lines 50-55).

12. As to claims 10, 25, 40, and 52, Naganuma et al. teaches further comprising evaluating the complete clock net to determine whether the results converge (see fig 1 element ST10 and fig29 element ST21 and ST13 col 12 lines 35-41).

13. As to claims 11, 26, 41, and 53, Naganuma et al. teaches wherein, if the results do not converge, the method further comprises: assuming that clock arrival times are those calculated for the simulated global clock net (see fig 1 element ST10 and fig29 element ST21 and ST13 col

12 lines 35-41); re-simulating at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net (see fig 1 element ST10 and fig29 element ST21 and ST13 col 12 lines 35-41); re-simulating the global clock net based in part on the simulated or re-simulated load of each of the plurality of local clock nets (see fig 1 element ST10 and fig29 element ST21 and ST13 col 12 lines 35-41); and combining the simulations and re-simulations to form the complete clock net (see fig 1 element ST10 and fig29 element ST21 and ST13 col 12 lines 35-41).

14. As to claims 12, 27, and 54, Naganuma et al. teaches wherein re-simulating at least one of the plurality of local clock nets comprises: re-simulating the at least one local clock net based on the layout, the component values, and the calculated clock arrival times (see fig 1 element ST10 and fig29 element ST21 and ST13 col 10 lines 35-41); and extracting a load of the at least one local clock net on the global clock net (see fig 1 element ST10 and fig29 element ST21 and ST13 col 10 lines 35-41).

15. As to claims 13, 28, and 55, Naganuma et al. teaches further comprising re-simulating at least a second of the plurality of local clock nets in parallel with the at least one local clock net (see fig 1 element ST10 and fig29 element ST21 and ST13 col 10 lines 55-68).

16. As to claims 14, 29, and 56, Naganuma et al. teaches wherein re-simulating the global clock net comprises: inserting the simulated or re-simulated loads of the plurality of local clock nets (see fig 1 element ST10 and fig29 element ST21 and ST11-14 col 12 lines 36-41); and re-simulating the global clock net based on the layout, the component values, and the simulated or re-simulated local clock net loads (see fig 1 element ST10 and fig29 element ST21 and ST11-14 col 12 lines 36-41).

17. As to claims 15, 30, 42, and 57, Naganuma et al. teaches further comprising storing the plurality of simulation and re-simulation results in a Clock Data Model (see fig 1 element ST10 and fig29 element ST21 and ST11-14 col 12 lines 36-41).

18. As to claims 58 (method), 63 (apparatus), 68 (apparatus), and 733 (computer readable medium), Naganuma et al. teaches a method of determining and analyzing clock insertion delays for a microprocessor design having grid-based clock distribution, the method comprising: partitioning the complete clock net into a global clock net and a plurality of local clock nets (see fig 5 col 7 lines 54-57 and fig 15 col 10 lines 20-23); simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net (see fig1 element ST10 and fig29 element ST21 and ST13 col 10 lines 55-68); simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets (see fig 1 element ST10 and fig29 element ST21 and ST13 col 10 lines 23-53); combining the plurality of simulations to form the complete clock net (see fig 1 element ST10 and fig29 element ST21 and ST11-14 col 12 lines 36-41); and analyzing the complete clock net to predict the clock skew for a given data transfer path (see col 7 lines 65 –67 and col 8 lines1-6 and col 11 lines 1-12).

19. As to claims 59, 64, 69, and 74, Naganuma et al. teaches wherein analyzing comprises: adjusting an insertion delay of the involved elements of the given data transfer path (see col 10 lines 10-14 and col 10 lines 33-42); and re simulating at least one local clock net involved in the given data transfer path (see fig 1 element ST10 and fig29 element ST21 and ST11-14 col 12 lines 36-41).

20. As to claims 60, 65, 70, and 75, Naganuma et al. teaches further comprising, when the at least one re-simulated local clock net is connected to at least one sub-local clock net, evaluating the clock arrival times to determine whether the sub-local clock net should be re-simulated (see fig 1 element ST10 and fig29 element ST21 and ST11-14 col 12 lines 36-41).

21. As to claims 61, 66, 71, and 76, Naganuma et al. teaches further comprising evaluating the at least one re-simulated clock net load to determine whether at least one higher clock net connected to the at least one re-simulated local clock net should be re-simulated (see fig 1 element ST10 and fig29 element ST21 and ST11-14 col 12 lines 36-41).

22. As to claims 62, 67, 72, and 77, Naganuma et al. teaches further comprising storing the plurality of simulation and re-simulation results in a Clock Data Model (see fig 1 element ST10 and fig29 element ST21 and ST11-14 col 12 lines 36-41).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is (703) 305-4855. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew Smith can be reached on (703) 308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3431 for regular communications and (703) 305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Binh Tat
Art Unit 2825
February 22, 2003

LEIGH M. GARRETSON
PATENT EXAMINER

Notice of References Cited

Application/Control No.	Applicant(s)/Patent Under Reexamination	
09/982,452	HARITSA ET AL.	
Examiner	Art Unit	Page 1 of 1
Binh C. Tat	2825	

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,917,729	06-1999	Naganuma et al.	716/10
	B	US-6,442,740	08-2002	Kanamoto et al.	716/6
	C	US-6,260,182	07-2001	Mohan et al.	716/12
	D	US-6,205,572	03-2001	Dupenloup, Guy	716/5
	E	US-5,864,487	01-1999	Merryman et al.	716/6
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Form PTO 1449 (Rev. 2-32) U.S. Department of Commerce Patent and Trademark Office

Atty. Docket No. SUN-P5403	Serial No. 09/982,452
Applicant: Manjunath D. Haritsa, et al.	
Filed: October 17, 2001	Group: 2182

Information Disclosure Statement by Applicant

(Use several sheets if necessary)

U.S. Patent Documents

Init.		Document No.	Date	Name	Class	Subclass	Filing Date
BT	A	5,239,215	8/24/93	Yamaguchi	307	480	11/20/92
BT	B	6,150,865	11/21/00	Fluxman et al.	327	292	7/9/99
BT	C	6,311,313	10/30/01	Camporese et al.	716	6	12/29/98

Foreign Documents

Init.		Document No.	Date	Country	Class	Subclass	Translation Yes	Translation No

Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)

Examiner [signature] Date Considered 02/21/03

Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include a copy of this form with the next communication to applicant.

Form PTO-1449 (Rev. 02-32) U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. SUN-P5403	Serial No. 09/982,452
Information Disclosure Statement by Applicant (Use several sheets if necessary)	Applicant: Manjunath D. Haritsa, et al.	
	Filed: October 17, 2001	Group: (to be assigned)

U.S. Patent Documents

Init.		Document No.	Date	Name	Class	Subclass	Filing Date
BT	A	5,911,063	6/8/99	Allen et al.	395	555	8/18/97
BT	B	5,923,188	7/13/99	Kametani et al.	326	93	6/12/96
BT	C	6,025,740	2/15/00	Fukuyama	326	93	9/3/93

Foreign Documents

Init.		Document No.	Date	Country	Class	Subclass	Translation Yes	Translation No

Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)

Examiner	Date Considered
	02/21/03

Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include a copy of this form with the next communication to applicant.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/982,452	10/17/2001	Manjunath D. Haritsa	SUN-P5403	7441

7590 07/14/2003

David B. Ritchie
Thelen Reid & Priest LLP
P.O. Box 640640
San Jose, CA 95164-0640

81173-671

EXAMINER
TAT, BINH C

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 07/14/2003

QA 10-14-03
LD 1-14-04

Please find below and/or attached an Office communication concerning this application or proceeding.

Missing 2 publications

Mail log_____ Date_____

CPI SB Date 7-24-03

Excel_____ Date_____

Office Action Summary

Application No.	Applicant(s)	
09/982,452	HARITSA ET AL.	
Examiner	**Art Unit**	
Binh C. Tat	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-77* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-77* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This office action is in response to application 09/982452 filed on 10/17/01.

Claims 1-77 remain pending in the application.

Response to Arguments

Applicant's arguments with respect to claims 1-77 have been considered but are persuasive in view of the new ground's of rejection.

Double Patenting

Claims 1, 16, 24, 31, 39, 43, 51 provisionally rejected under 35 U.S.C. 101 as claiming the same invention as claiming the same invention as that of claims 1-26 of copending Application No. 09/982459. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-77 provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-49 of copending Application No. 09/982458. Although the conflicting claims are not identical, they are not patentably distinct

from each other because the removal unnecessary steps in an invention is an obvious development in the art.

Claim Rejections - 35 USC § 103

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Rejection of Claims 1-77

4. Claims 1-77 are rejected under 35 U.S.C. 103(a) as being unpatentable over Camporese et al. ("Camporese"), U.S. Patent 6,205,571 and Graef, U.S. Patent 6,305,001. Camporese discloses a clock tree distribution network for distributing a clock signal across a

chip involving clock skew analysis. Although Camporese suggests Applicants' limitations, Camporese does not disclose a specific system for implementing the method. Graef also discloses a clock tree distribution planning method and additionally discloses a system for implementing the method that is a typical system used in IC designs. Graef further states that the system disclosed represents "one of many suitable computer platforms for implementing the method." (col. 15, II. 47-50). Both Camporese and Graef disclose a method involving a clock distribution network.. However, Graef details the system that would be necessary to implement methods involving clock distribution networks in general. It therefore would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to use the system of Graef, or some similar system configuration, to implement the Camporese method.

5. Pursuant to claims 1, 16, 31, and 43 which recites a Clock Data Model (Fig. 2 illustrates this limitation; also, col. 3, II. 48-50 discloses a clock-related electrical simulation model) for use with a method of determining clock insertion delays for a microprocessor design having grid-based clock distribution comprising,

partitioning the complete clock net into a global clock net (the first level wiring networks, e.g. Figure 2, #201; reference the Fig. 2 description at col. 4, II. 25-28) and a plurality of local clock nets (the second level of tree wires, e.g. Figure 2, #203; reference the Figure 2 description at col. 4, II. 28-31);

simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net: col. 12, II. 12-23 wherein the twig wiring represents the local clock nets; additionally, the Nsector electrical lists comprise the loading for the plurality of local clock nets;.

simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets: col. 12, II. 12-23 wherein the twig wiring represents the local clock nets; combining the plurality of simulations to form the complete clock net: col. 11, II. 33-50;

6. Pursuant to claims 2, 17, 32, and 44 wherein partitioning comprises breaking the complete clock net into equal sized parts according to rectangular grid coordinates: Figure 2 illustrates this limitation.

7. Pursuant to claim 3, 18, 33 and 45 wherein the method further comprises breaking at least one of the plurality of local clock nets down into at least one sub-local clock net: col. 4, II. 28-31 suggests the existence of sub-local clock nets depending on the embodiment.

8. Pursuant to claim 4, 19, 34, and 46 wherein the method further comprises simulating the at least one sub-local clock net prior to simulating the corresponding local clock net: Fig. 7, step 735; col. 9, II. 60-64.

9. Pursuant to claims 5, 20, 35, and 47 wherein at least two of the plurality of local clock nets are simulated in parallel: Creation of isolated net lists which represent local clock nets and are treated in parallel for tuning or simulation purposes, col. 9, II. 8-27; see also col. 9, II. 61-67 which discloses parallel tuning or simulation.

10. Pursuant to claims 6, 21, 36, 48 wherein simulating the clock nets comprises extracting a layout of the local clock net and the conductors routed above and through the local clock net from a microprocessor network database: the creation of the electrical netlist suggests this limitation, col. 6, II. 10-65;

extracting component values of the elements of the local clock net from the microprocessor network database: col. 6, II. 48-65;

simulating the local clock net based on the layout and the component values: col. 6, II. 48-65;

extracting a load of the local clock net on the global clock net: col. 6, II. 48-65.

11. Pursuant to claims 7, 22, 37, and 49 wherein simulating the local clock net comprises assuming that the clock arrival times form the global clock net will be simultaneous at all points where the local clock net is connected to the global clock net: col. 9, II. 35-43.

12. Pursuant to claims 8, 23 38, and 50wherein simulating the global clock net comprises extracting the layout of the global clock net from a microprocessor network database: the creation of the electrical netlist, col. 6, II. 10-65, details the layout connections;

extracting component values of the elements of the global clock from the microprocessor network database: col. 6, II. 48-65;

inserting the simulated loads of the plurality of local clock nets: col. 6, II. 48-54; see also col. 7, II. 13-15;

simulating the global clock net based on the layout, the component values, and the simulated local clock net loads: col. 6, II. 48-65.

13. Pursuant to claims 9, 24, 39 and 51 which further comprises storing the plurality of simulations in the Clock Data Model: col. 11, II. 19-22, wherein the tuned netlist represents the CDM with stored simulations.

14. Pursuant to claims 10, 25, 40 and 52 which further comprises evaluating the complete clock net to determine whether the results converge: col. 9, II. 35-60, wherein the true point load response matrix is checked against the smoothed point load response matrix which has calculations of clock signal arrival times.

15. Pursuant to claims 11, 26, 41,and 53 wherein if the results do not converge, replacing the clock arrival times with those calculated for the simulated global clock net: col. 9, lines 4756;

re-simulating one of the plurality of local clock nets to generate a load for the local and global clock net: col. 12, II. 12-23;

re-simulating the global clock net based on the simulated or re-simulated load of each of the plurality of local clock nets: col. 12, II. 12-13 wherein the twig wiring represents the local clock nets.

combining the simulations and re-simulations to form the complete net: col. 11, II. 33-50.

16. Pursuant to claims 12, 27 and 54 wherein re-simulating the local clock net comprises resimulating the local clock net based on the layout, the component values, and the calculated clock arrival times: col. 6, II. 48-65;

extracting a load of the at least one local clock net on the global clock net: col. 6, II. 48-65.

17. Pursuant to claims 13, 28, and 55 wherein the method comprises re-simulating at least a second of the plurality of local clock nets in parallel with the at least one local clock net:

18. Pursuant to claims 14, 29 and 56 wherein re-simulating the global clock net comprises inserting the simulated or re-simulated loads of the plurality of local clock nets (col. 6, II. 48-54; see also col. 7, II. 13-15); and

re-simulating the global clock net based on the layout, the component values, and the simulated or re-simulated local clock net loads: col. 6, II. 48-65.

19. Pursuant to claim 15, 30, 42 and 57, wherein the method further comprises storing the plurality of re-simulations in the Clock Data Model: col. 11, II. 19-22.

20. Pursuant to Claim 58, 63, 68 and 73 which recites a Clock Data Model (Fig. 2 illustrates this limitation; also, col. 3, II. 48-50 discloses a clock-related electrical simulation model) for use with a method of determining clock insertion delays for a microprocessor design having grid-based clock distribution comprising,

partitioning the complete clock net into a global clock net (the first level wiring networks, e.g. Figure 2, #201; reference the Fig. 2 description at col. 4, II. 25-28) and a plurality of local clock nets (the second level of tree wires, e.g. Figure 2, #203; reference the Figure 2 description at col. 4, II. 28-31);

simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net: col. 12, II. 12-23 wherein the twig wiring represents the local clock nets; additionally, the Nsector electrical lists comprise the loading for the plurality of local clock nets;.

simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets: col. 12, II. 12-23 wherein the twig wiring represents the local clock nets;

combining the plurality of simulations to form the complete clock net: col. 11, II. 33-50;

analyzing the complete clock net to predict the clock skew for a given data transfer path: black ground and fig 2-5 col 4-6.

21. Pursuant to claim 59, 64, 69, and 74 wherein analyzing comprises: adjusting an insertion delay of the involved elements of the given data transfer path: black ground and fig 2-5 col 4-6; and re simulating at least one local clock net involved in the given data transfer ; black ground and fig 2-5 col 4-6.

22. Pursuant to claim 60-62, 65-67, and 75-77 further comprising, when the at least one re-simulated local clock net is connected to at least one sub-local clock net, evaluating the clock arrival times to determine whether the sub-local clock net should be re-simulated: black ground and fig 2-5 col 4-6.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is (703) 305-4855. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew Smith can be reached on (703) 308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3431 for regular communications and (703) 305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Binh Tat
Art Unit 2825
June 30, 2003

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Notice of References Cited

Application/Control No.	Applicant(s)/Patent Under Reexamination	
09/982,452	HARITSA ET AL.	
Examiner	Art Unit	Page 1 of 1
Binh C. Tat	2825	

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,205,571	03-2001	Camporese et al.	716/2
	B	US-6,305,001	10-2001	Graef, Stefan	716/12
	C	US-6,311,313	10-2001	Camporese et al.	716/6
	D	US-6,053,950	04-2000	Shinagawa, Naoko	716/2
	E	US-6,150,865	11-2000	Fluxman et al.	327/292
	F	US-6,204,713	03-2001	Adams et al.	327/295
	G	US-2003/0074175	04-2003	Haritsa et al.	703/19
	H	US-2003/0074643	04-2003	Schmitt et al.	716/6
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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811173-346 ← wrong #

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/982,452	10/17/2001	Manjunath D. Haritsa	SUN-P5403	7441

7590 12/17/2003

EXAMINER
TAT, BINH C

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 12/17/2003

David B. Ritchie
Thelen Reid & Priest LLP
P.O. Box 640640
San Jose, CA 95164-0640

Final OA 2-17-04
APP 3-17-04
LD 6-17-04

Please find below and/or attached an Office communication concerning this application or proceeding.

Mail log_____ Date_____
DOCK.
CPI_____ Date DEC 23 2003
Excel_____ Date_____

Application No.	Applicant(s)	
09/982,452	HARITSA ET AL.	
Examiner	**Art Unit**	
Binh C. Tat	2825	

Office Action Summary

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-77* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-77* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This is a response to the response filed on 09/29/03. The applicant argument regarding Haritsa, Manjunath are not persuasive; therefore, all the rejections based on Haritsa, Manjunath are retained and repeated for the following reasons.

Terminal Disclaimer

The terminal disclaimer filed on 09/29/03 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of any patent granted on Application Number 09/982459 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Claim Rejections - 35 USC § 103

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have

been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Rejection of Claims 1-77

4. Claims 1-77 are rejected under 35 U.S.C. 103(a) as being unpatentable over Camporese et al. ("Camporese"), U.S. Patent 6,205,571 and Graef, U.S. Patent 6,305,001. Camporese discloses a clock tree distribution network for distributing a clock signal across a chip involving clock skew analysis. Although Camporese suggests Applicants' limitations, Camporese does not disclose a specific system for implementing the method. Graef also discloses a clock tree distribution planning method and additionally discloses a system for implementing the method that is a typical system used in IC designs. Graef further states that the system disclosed represents "one of many suitable computer platforms for implementing the method." (col. 15, II. 47-50). Both Camporese and Graef disclose a method involving a clock distribution network.. However, Graef details the system that would be necessary to implement methods involving clock distribution networks in general. It therefore would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to use the system of Graef, or some similar system configuration, to implement the Camporese method.

5. Pursuant to claims 1, 16, 31, and 43 which recites a Clock Data Model (Fig. 2 illustrates this limitation; also, col. 3, II. 48-50 discloses a clock-related electrical simulation model) for use with a method of determining clock insertion delays for a microprocessor design having grid-based clock distribution comprising,

partitioning the complete clock net into a global clock net (the first level wiring networks, e.g. Figure 2, #201; reference the Fig. 2 description at col. 4, II. 25-28) and a plurality of local clock nets (the second level of tree wires, e.g. Figure 2, #203; reference the Figure 2 description at col. 4, II. 28-31);

simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net: col. 12, II. 12-23 wherein the twig wiring represents the local clock nets; additionally, the Nsector electrical lists comprise the loading for the plurality of local clock nets;.

simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets: col. 12, II. 12-23 wherein the twig wiring represents the local clock nets;

combining the plurality of simulations to form the complete clock net: col. 11, II. 33-50;

6. Pursuant to claims 2, 17, 32, and 44 wherein partitioning comprises breaking the complete clock net into equal sized parts according to rectangular grid coordinates: Figure 2 illustrates this limitation.

7. Pursuant to claim 3, 18, 33 and 45 wherein the method further comprises breaking at least one of the plurality of local clock nets down into at least one sub-local clock net: col. 4, II. 28-31 suggests the existence of sub-local clock nets depending on the embodiment.

8. Pursuant to claim 4, 19, 34, and 46 wherein the method further comprises simulating the at least one sub-local clock net prior to simulating the corresponding local clock net: Fig. 7, step 735; col. 9, II. 60-64.

9. Pursuant to claims 5, 20, 35, and 47 wherein at least two of the plurality of local clock nets are simulated in parallel: Creation of isolated net lists which represent local clock nets and

are treated in parallel for tuning or simulation purposes, col. 9, II. 8-27; see also col. 9, II. 61-67 which discloses parallel tuning or simulation.

10. Pursuant to claims 6, 21, 36, 48 wherein simulating the clock nets comprises extracting a layout of the local clock net and the conductors routed above and through the local clock net from a microprocessor network database: the creation of the electrical netlist suggests this limitation, col. 6, II. 10-65;

extracting component values of the elements of the local clock net from the microprocessor network database: col. 6, II. 48-65;

simulating the local clock net based on the layout and the component values: col. 6, II. 48-65;

extracting a load of the local clock net on the global clock net: col. 6, II. 48-65.

11. Pursuant to claims 7, 22, 37, and 49 wherein simulating the local clock net comprises assuming that the clock arrival times form the global clock net will be simultaneous at all points where the local clock net is connected to the global clock net: col. 9, II. 35-43.

12. Pursuant to claims 8, 23 38, and 50wherein simulating the global clock net comprises extracting the layout of the global clock net from a microprocessor network database: the creation of the electrical netlist, col. 6, II. 10-65, details the layout connections;

extracting component values of the elements of the global clock from the microprocessor network database: col. 6, II. 48-65;

inserting the simulated loads of the plurality of local clock nets: col. 6, II. 48-54; see also col. 7, II. 13-15;

simulating the global clock net based on the layout, the component values, and the simulated local clock net loads: col. 6, II. 48-65.

13. Pursuant to claims 9, 24, 39 and 51 which further comprises storing the plurality of simulations in the Clock Data Model: col. 11, II. 19-22, wherein the tuned netlist represents the CDM with stored simulations.

14. Pursuant to claims 10, 25, 40 and 52 which further comprises evaluating the complete clock net to determine whether the results converge: col. 9, II. 35-60, wherein the true point load response matrix is checked against the smoothed point load response matrix which has calculations of clock signal arrival times.

15. Pursuant to claims 11, 26, 41,and 53 wherein if the results do not converge, replacing the clock arrival times with those calculated for the simulated global clock net: col. 9, lines 4756;

re-simulating one of the plurality of local clock nets to generate a load for the local and global clock net: col. 12, II. 12-23;

re-simulating the global clock net based on the simulated or re-simulated load of each of the plurality of local clock nets: col. 12, II. 12-13 wherein the twig wiring represents the local clock nets.

combining the simulations and re-simulations to form the complete net: col. 11, II. 33-50.

16. Pursuant to claims 12, 27 and 54 wherein re-simulating the local clock net comprises resimulating the local clock net based on the layout, the component values, and the calculated clock arrival times: col. 6, II. 48-65;

extracting a load of the at least one local clock net on the global clock net: col. 6, II. 48-65.

17. Pursuant to claims 13, 28, and 55 wherein the method comprises re-simulating at least a second of the plurality of local clock nets in parallel with the at least one local clock net:

18. Pursuant to claims 14, 29 and 56 wherein re-simulating the global clock net comprises inserting the simulated or re-simulated loads of the plurality of local clock nets (col. 6, II. 48-54; see also col. 7, II. 13-15); and

re-simulating the global clock net based on the layout, the component values, and the simulated or re-simulated local clock net loads: col. 6, II. 48-65.

19. Pursuant to claim 15, 30, 42 and 57, wherein the method further comprises storing the plurality of re-simulations in the Clock Data Model: col. 11, II. 19-22.

20. Pursuant to Claim 58, 63, 68 and 73 which recites a Clock Data Model (Fig. 2 illustrates this limitation; also, col. 3, II. 48-50 discloses a clock-related electrical simulation model) for use with a method of determining clock insertion delays for a microprocessor design having grid-based clock distribution comprising,

partitioning the complete clock net into a global clock net (the first level wiring networks, e.g. Figure 2, #201; reference the Fig. 2 description at col. 4, II. 25-28) and a plurality of local clock nets (the second level of tree wires, e.g. Figure 2, #203; reference the Figure 2 description at col. 4, II. 28-31);

simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net: col. 12, II. 12-23 wherein the twig wiring represents the local clock nets; additionally, the Nsector electrical lists comprise the loading for the plurality of local clock nets;.

simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets: col. 12, II. 12-23 wherein the twig wiring represents the local clock nets;

combining the plurality of simulations to form the complete clock net: col. 11, II. 33-50;

analyzing the complete clock net to predict the clock skew for a given data transfer path: black ground and fig 2-5 col 4-6.

21. Pursuant to claim 59, 64, 69, and 74 wherein analyzing comprises: adjusting an insertion delay of the involved elements of the given data transfer path: black ground and fig 2-5 col 4-6; and re simulating at least one local clock net involved in the given data transfer; black ground and fig 2-5 col 4-6.

22. Pursuant to claim 60-62, 65-67, and 75-77 further comprising, when the at least one re-simulated local clock net is connected to at least one sub-local clock net, evaluating the clock arrival times to determine whether the sub-local clock net should be re-simulated: black ground and fig 2-5 col 4-6.

Remarks

Applicant's response and remarks filed on 09/29/03 have been carefully review. Applicant's arguments have been fully considered but they are not persuasive. Key argument and their response related to the claims are listed as below:

23. The prior art (Camporese et al. US 6205571) does teach "a grid-based clock distribution" (see fig1-6 col 4 lines 40-59).

24. The prior art (Camporese et al. US 6205571) does teach "a layout of the local clock net and the conductors routed above and through the local clock net" (see fig 2 and fig 7 col 6 lines 10-43 fig 2 show how to layout the local clock net).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

25. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is (703) 305-4855. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew Smith can be reached on (703) 308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3431 for regular communications and (703) 305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

BINH TAT
Art Unit 2825
December 15, 2003

VUTHE SIEK
PRIMARY EXAMINER